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ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

6 Solutions to Case Studies and Exercises Case Study 1: Optimizing Cache Performance via Advanced Techniques 2.1 a. Each element is 8B. Since a 64B cacheline has 8 elements, and each column access will result in fetching a new line for the non-ideal matrix, we need a minimum of 8x8 (64 elements) for each matrix.

Computer architecture, a quantitative approach (solution ...

EXAM 1 SOLUTIONS Assume we would like to use the exact same solution (history buffer) for executing a store instruction to memory. Why is this difficult to do? It is difficult to UNDO the effect of a store instruction. Another processor might read and use the value supplied by the store instruction before the store is undone.

EXAM 1 SOLUTIONS - Electrical and Computer Engineering

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pair of CPUs to the network and implemented the cache coherence protocol. This ASIC consisted of about 900K gates, running at 100 MHz.

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